AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A printed circuit board, comprising:

a first power plane layer including a first segment for inputting current, a second segment for outputting current and a third segment for connecting said first and second segments, wherein electronic components are physically coupled only to said first and second segments; and

a first pair of conductive vias each coupled to different points on said third segment, wherein a current transferred from said first segment to said second segment is determined by a potential difference and a resistance between said first pair of conductive vias.

2. (Original) The printed circuit board according to claim 1, wherein said first segment includes a plurality of conductive vias designed to obtain linear current flow between said first segment and said second segment.

3. (Withdrawn) The printed circuit board according to claim 1, wherein a first current source mounted on an external layer is coupled to said first segment.

4. (Withdrawn) The printed circuit board according to claim 3, wherein said first pair of conductive vias are coupled to a first current sharing controller mounted on an external layer with feedback provided to said first current source to optimize output current balancing.

5. (Withdrawn) The printed circuit board according to claim 3 further comprising a fourth segment for inputting current and a fifth segment for outputting current coupled to a second current source mounted on said external layer and coupled in parallel with said first current source.

6. (Withdrawn) The printed circuit board according to claim 5, wherein a second pair of conductive vias are coupled to a second current sharing controller with feedback provided to said second current source to optimize parallel output current balancing.

7. (Withdrawn) The printed circuit board according to claim 3, wherein said first current source mounted on said external layer is coupled to said first power plane layer and a second current

source mounted on said external layer is coupled to a second power plane layer with said first current source and said second current source connected in parallel.

8. (Withdrawn) The printed circuit board according to claim 4, wherein said first current sharing controller is coupled to said first current source and a second current sharing controller mounted on said external layer is coupled to a second current source.

9. (Withdrawn) The printed circuit board according to claim 7, wherein said first power plane layer is coupled to said second power plane layer by a plurality of vias.

10. (Currently Amended) [[1he]] The printed circuit board according to claim 1, wherein said first segment comprises a rectangular geometry.

11. (Withdrawn) The printed circuit board according to claim 1, wherein said first segment comprises a pseudo-random shaped geometry.

12. (Original) The printed circuit board according to claim 1, wherein said first segment is electrically characterized for linear current flow.

13. (Original) The printed circuit board according to claim 1, wherein said third segment is capable of carrying current greater than about 20 amperes.

14. (Original) The printed circuit board according to claim 13, wherein said third segment is capable of carrying current from about 20 to about 40 amperes.

15. (Original) The printed circuit board according to claim 1, wherein said third segment is capable of carrying current less than about 20 amperes.

16. (Original) The printed circuit board according to claim 1, wherein a lookup table is utilized for current derivation correlated with the difference in potential measured at said first pair of conductive vias.

17. (Withdrawn) A method for measuring current on a printed circuit board, the method comprising the steps of:

providing a first power plane layer including a first segment for inputting current, a second segment for outputting current and a third segment for connecting said first and second segments;

providing a first pair of conductive vias each coupled to different points on said third segment; and

determining a current transferred from said first segment to said second segment from a potential difference and a resistance between said pair of conductive vias.

18. (Withdrawn) The method according to claim 17 further comprising the step of providing a plurality of conductive vias designed to obtain linear current flow between said first segment and said second segment.

19. (Withdrawn) The method according to claim 17, wherein said resistance comprises a sheet resistance of a portion of said third segment.

20. (Withdrawn) The method according to claim 17 further comprising the step of providing a first current sharing controller on an external layer coupled to said conductive vias with feedback provided to a first current source to optimize output current balancing.

21. (New) The printed circuit board according to claim 1, wherein each of said first pair of conductive vias comprises an end portion which terminates on said third segment and another end portion which terminates on a pad.